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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,141	12/15/2005	Jun-Ichi Okamura	1032-0002WOUS	5031

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EXAMINER	
CHENG, DIANA	
ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,141	OKAMURA, JUN-ICHI	
	Examiner	Art Unit	
	Diana J. Cheng	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/27/2005,12/27/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 5 and 10 recites the limitation "equal bias potentials are applied to gate nodes of the two N-channel MOS transistors in the first current supply circuit and the gate nodes of the two P-channel MOS transistors in the second current supply circuit" in lines 2-6. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this examination, the claim will be read as "equal bias potentials are applied to gate nodes of the two N-channel MOS transistors in the first differential circuit and the gate nodes of the two P-channel MOS transistors in the second differential circuit."

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koh (US 6,320,422 B1) as cited in the IDS filed 04/27/2005 and Morishita (US 6,963,230 B2).

Re claim 1, Koh discloses a differential circuit in Fig. 3 including

a differential amplifier circuit having

a differential element provided in a signal input circuit (302), a constant current source connected to the differential element (304), and loads respectively connected to the differential element (312 and 310); and

a source follower circuit (326 or 328) that outputs a differential voltage (OUT+ and OUT-) based on voltage drops developing across the loads (308 and 306), but does not teach the rest of the claim.

Morishita teaches in Fig. 2 a circuit comprising a current supply circuit that supplies a given current to the loads connected in series with the differential element when the differential element is off (DRM).

Koh teaches a circuit where low voltage swing, low gain, and high bandwidth are preserved. Morishita further teaches (Col. 1 lines 50-55), the "voltage-drop system is also characterized in that, when the down-converted voltage is set constant at a level sufficiently lower than the external power supply voltage, the constant level is maintained even in the event of variation in the external power supply voltage to allow stable operation of internal circuitry." Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the control system as demonstrated in Fig. 1 and Fig. 2 of Morishita, to the circuit as shown in Koh, for the purpose of maintaining a constant level, even in the event of variation in the external power supply voltage to allow stable operation of internal circuitry.

Re claim 2, Koh discloses a differential circuit including

a first differential amplifier circuit having

a first differential element provided in a signal input circuit (302), a first constant current source connected to the first differential element (304), and

a first and a second loads respectively connected to the first differential element (312 and 310);

a second differential amplifier circuit having

a second differential element provided in the signal input circuit (314), a second constant current source connected to the second differential element (316), and

a third and a fourth loads respectively connected to the second differential element (324 and 322);

a first source follower circuit that outputs a first differential voltage based on voltage drops developing across the first and second loads (326); and

a second source follower circuit that outputs a second differential voltage based on the voltage drops developing across the third and fourth loads (328), but does not teach the rest of the claim.

Morishita teaches in Fig. 13 a circuit comprising a first current supply circuit that supplies a given current to the first and second loads when the first differential element is off (DRM); and

a second current supply circuit that supplies the given current to the third and fourth loads when the second differential element is off (DRS).

It would be obvious to one of ordinary skill in the art to combine Koh and Morishita, for the same reasons as stated in Claim 1.

Re claim 3, Koh and Morishita, as a whole, teach the differential circuit as claimed in claim 2, wherein Koh further teaches each of the first and the second source follower circuits is a complementary follower circuit having two MOS transistors (Fig. 4, 438, 440, 434, and 432).

Re claim 4, Koh and Morishita, as a whole, teach the differential circuit as claimed in claim 2, wherein Koh further teaches:

the first differential element includes two N-channel MOS transistors (404 and 402);

the first current supply circuit is connected to gates of the two N-channel MOS transistors (in+ and in-);

the second differential element includes two P-channel MOS transistors (426 and 428); and

the second current supply circuit is connected to gates of the two P-channel MOS transistors (in+ and in-).

Re claim 5, Koh and Morishita, as a whole, teach the differential circuit as claimed in claim 4, wherein equal bias potentials are applied to gate nodes of the two N-channel MOS transistors in the first differential circuit and the gate nodes of the two P-channel MOS transistors in the second differential circuit (Koh teaches in+ and in-, which are differential and bias inputs.)

Claim 6 has been analyzed and rejected in reference to claim 1, where in a receiving device contains the differential circuit of claim 1 (Col. 1, lines 8-9, "suitable for low voltage differential signaling", where signaling comprises of transmitting and receiving, thereby equivalent to having the differential circuit used in a receiving device).

Claim 7 has been analyzed and rejected in reference to claim 2, where in a receiving device contains the differential circuit of claim 2 (Col. 1, lines 8-9, "suitable for low voltage differential signaling", where signaling comprises of transmitting and receiving, thereby equivalent to having the differential circuit used in a receiving device).

Claim 8 has been analyzed and rejected in reference to claims 7 and 3.

Claim 9 has been analyzed and rejected in reference to claims 7, 8, and 4.

Claim 10 has been analyzed and rejected in reference to claims 9 and 5.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ewen et al. (US 6,207,685 B1) teaches an output buffer provides a stable, predetermined low voltage differential over power supply, temperature, and process variations yet has a high speed of operation. More particularly, a data path of an output buffer includes an emitter-coupled differential amplifier followed by an output section of two level-shifting emitter followers. A predetermined operating current biases the differential amplifier for unsaturated operation and a reference current biases the output section for unsaturated operation. The data path remains unencumbered by compensation circuitry to preserve high-speed operation. Instead, a voltage compensator biases the differential amplifier to compensate, at least in part, for variations in a supply voltage. In addition, a variable biasing current to the voltage compensator with a predetermined temperature coefficient may further temperature compensate the differential amplifier. In addition to such "upstream" compensation, the output buffer may further include "downstream" temperature compensation by the addition of a V.sub.BE multiplier circuit to the reference current biasing of the output section. Additional temperature and level-shifting compensation may also be achieved through cascading a plurality of buffer stages.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Diana J. Cheng whose telephone number is (571) 270-1197. The examiner can normally be reached on Monday-Friday, 7:30am-5:00 pm, alt. Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJC
06/09/2007

Kenneth B. Wells
Primary Examiner